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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/073,847	02/11/2002	Matthias Stecher	WMP-IFT-699	6635

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LERNER AND GREENBERG, P.A.
Post Office Box 2480
Hollywood, FL 33022-2480

EXAMINER

PRENTY, MARK V

ART UNIT

PAPER NUMBER

2822

10

DATE MAILED: 03/05/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/073,847

Applicant(s)

STECHER et al.

Examiner

Prenty

Art Unit

2822



-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE three MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on Feb 19, 2003.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-14 is/are pending in the application.
- 4a) Of the above, claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1, 2, and 4-6 is/are rejected.
- 7) ☒ Claim(s) 3 and 7-14 is/are objected to.
- 8) ☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
*See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).
a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892) 4) ☐ Interview Summary (PTO-413) Paper No(s). _____
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) 5) ☐ Notice of Informal Patent Application (PTO-152)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s). _____ 6) ☐ Other:

This Office Action is in response to the papers filed February 19, 2003.

Claims 1, 2, 5 and 6 are rejected under 35 U.S.C. §103(a) as being unpatentable over Letavic et al. (United States Patent 6,221,737, already of record) together with Assaderaghi et al. (United States Patent 6,121,661, already of record).

With respect to independent claim 1, Letavic et al. disclose a semiconductor component (see the entire reference, particularly Fig. 1), comprising: a semiconductor substrate 100; an insulation layer 102 on said semiconductor substrate, said insulating layer having a thickness of between 50 nm and 200 nm (see the paragraph bridging columns 3 and 4); a semiconductor layer 104 configured on said insulation layer; a first doped terminal zone 108 and a second doped terminal zone 116 formed in said semiconductor layer; and a drift zone 110 formed in said semiconductor layer; said drift zone formed between said first doped terminal zone and said second doped terminal zone.

The difference between Letavic et al's semiconductor component and claim 1's semiconductor component is at least one of claim 1's first and second doped terminal zones directly adjoins the semiconductor substrate.

Assaderaghi et al. teach connecting the source and drain regions of a MOSFET formed in an SOI (silicon on insulator) configuration to the underlying semiconductor substrate, in order to provide ESD (electrostatic discharge) protection and improved heat dissipation (see the entire reference, particularly Fig. 4A).

It would have been obvious to one skilled in this art to connect Letavic et al's source and drain regions 108 and 116 (i.e., its first and second doped terminal zones) to underlying substrate 100, in order to provide Letavic et al's semiconductor component with ESD protection and improved heat dissipation, as taught by Assaderaghi et al.

Claim 1 is thus rejected under 35 U.S.C. §103(a) as being unpatentable over Letavic et al. together with Assaderaghi et al.

With respect to dependent claim 2, as stated above with respect to independent claim 1, it would have been obvious to one skilled in this art to connect Letavic et al's source and drain regions 108 and 116 (i.e., its first and second doped terminal zones) to underlying substrate 100, in order to provide Letavic et al's semiconductor component with ESD protection and improved heat dissipation, as taught by Assaderaghi et al..

Claim 2 is thus rejected under 35 U.S.C. §103(a) as being unpatentable over Letavic et al. together with Assaderaghi et al.

With respect to dependent claim 5, Letavic et al's semiconductor component further comprises a depletion zone 106 configured between said second terminal zone 116 and said drift zone 110; said depletion zone having a conduction type; and said first terminal zone 108 and said second terminal zone 116 having a conduction type that is complementary to said conduction type of said depletion zone.

Claim 5 is thus rejected under 35 U.S.C. §103(a) as being unpatentable over Letavic et al. together with Assaderaghi et al.

With respect to dependent claim 6, Letavic et al's first terminal zone 108 has a conduction type; and its drift zone 110 has a conduction type that is equivalent to the conduction type of said first terminal zone.

Claim 6 is thus rejected under 35 U.S.C. §103(a) as being unpatentable over Letavic et al. together with Assaderaghi et al.

Claims 1, 2 and 4 are rejected under 35 U.S.C. §103(a) as being unpatentable over Merchant (newly cited United States Patent 5,648,671) together with Assaderaghi et al. (United States Patent 6,121,661, already of record).

With respect to independent claim 1, Merchant discloses a semiconductor component (see Fig. 1), comprising: a semiconductor substrate 100; an insulation layer 102 on said semiconductor substrate, said insulating layer having a thickness of between 50 nm and 200 nm (see column 2, lines 47-50); a semiconductor layer 104 configured on said insulation layer; a first doped terminal zone 108 and a second doped terminal zone 106 formed in said semiconductor layer; and a drift zone 110 formed in said semiconductor layer; said drift zone formed between said first doped terminal zone and said second doped terminal zone.

The difference between Merchant's semiconductor component and claim 1's semiconductor component is at least one of claim 1's first and second doped terminal zones directly adjoins the semiconductor substrate.

Assaderaghi et al. teach connecting the active regions of a device formed in an SOI (silicon on insulator) configuration to the underlying semiconductor substrate, in order to provide ESD (electrostatic discharge) protection and improved heat dissipation (see the entire reference, particularly Fig. 4A).

It would have been obvious to one skilled in this art to connect Merchant's cathode and anode regions 108 and 106 (i.e., its first and second doped terminal zones) to underlying substrate 100, in order to provide Merchant's semiconductor component with ESD protection and improved heat dissipation, as taught by Assaderaghi et al.

Claim 1 is thus rejected under 35 U.S.C. §103(a) as being unpatentable over Merchant together with Assaderaghi et al.

With respect to dependent claim 2, as stated above with respect to independent claim 1, it would have been obvious to one skilled in this art to connect Merchant's cathode and anode regions 108 and 106 (i.e., its first and second doped terminal

zones) to underlying substrate 100, in order to provide Merchant's semiconductor component with ESD protection and improved heat dissipation, as taught by Assaderaghi et al..

Claim 2 is thus rejected under 35 U.S.C. §103(a) as being unpatentable over Merchant together with Assaderaghi et al.

With respect to dependent claim 4, Merchant's second terminal zone 106 is of a complementary conduction type (p-type) with respect to said (n-type) first terminal zone 108 (see column 2, lines 55-61).

Claim 4 is thus rejected under 35 U.S.C. §103(a) as being unpatentable over Merchant together with Assaderaghi et al.

Claim 3 is objected to as being dependent on a rejected base claim (i.e., claim 3 would be allowable over the prior art of record if claim 3 were amended to further include all the limitations of independent claim 1 and dependent claim 2).

Claim 7 is objected to as being dependent on a rejected base claim (i.e., claim 7 would be allowable over the prior art of record if claim 7 were amended to further include all the limitations of independent claim 1).

Claim 8 is objected to as being dependent on a rejected base claim (i.e., claim 8 would be allowable over the prior art of record if claim 8 were amended to further include all the limitations of independent claim 1 and dependent claim 7).

Claim 9 is objected to as being dependent on a rejected base claim (i.e., claim 9 would be allowable over the prior art of record if claim 9 were amended to further include all the limitations of independent claim 1 and dependent claim 7).

Claim 10 is objected to as being dependent on a rejected base claim (i.e., claim 10 would be allowable over the prior art of record if claim 10 were amended to further include all the limitations of independent claim 1 and dependent claim 7).

Claim 11 is objected to as being dependent on a rejected base claim (i.e., claim 11 would be allowable over the prior art of record if claim 11 were amended to further include all the limitations of independent claim 1, dependent claim 7 and dependent claim 10).

Claim 12 is objected to as being dependent on a rejected base claim (i.e., claim 12 would be allowable over the prior art of record if claim 12 were amended to further include all the limitations of independent claim 1, dependent claim 7 and dependent claim 10).

Claim 13 is objected to as being dependent on a rejected base claim (i.e., claim 13 would be allowable over the prior art of record if claim 13 were amended to further include all the limitations of independent claim 1, dependent claim 7 and dependent claim 10).

Claim 14 is objected to as being dependent on a rejected base claim (i.e., claim 14 would be allowable over the prior art of record if claim 14 were amended to further include all the limitations of independent claim 1).

The applicant's arguments with respect to the maintained rejection of claims 1, 2, 5 and 6 under 35 U.S.C. §103(a) as being unpatentable over Letavic et al. together with Assaderaghi et al. are not persuasive for at least two reasons.

First, the applicant only discusses the references separately and fails to address how those references are combined in said 35 U.S.C. §103(a) rejection.

Furthermore, the obvious Letavic et al. / Assaderaghi et al. semiconductor device includes the claim 1 limitations emphasized on page 4 of the response, as evidenced by the statement of the rejection (see above). It is worth repeating here that Letavic et al.'s insulating layer 102 has a thickness between 50 nm and 200 nm (again, see Letavic et al. at the paragraph bridging columns 3 and 4).

The proposed drawing change has been approved by the examiner.

The formal copy of the proposed drawing change has been approved by the draftsperson.

Registered practitioners can telephone the examiner at (703) 308-4939. Any voicemail message left for the examiner must include the name and registration number of the registered practitioner calling, and the application's PTO Serial Number. Technology Center 2800's general telephone number is (703) 308-0956.

Mark Prentz
2009/07/13